IN THE TITLE

Please amend the Title Of The Invention as follows.

~~SEMICONDUCTOR DEVICE AND FABRICATING~~ METHOD ~~THEREOF~~ OF MANUFACTURING SEMICONDUCTOR DEVICE FEATURING FORMATION OF CONDUCTIVE PLUGS

IN THE SPECIFICATION

Please amend the following paragraphs as shown below.

[0023] As shown in Fig. 2C, the photoresist layer ~~215~~ 216 is removed. A portion of the exposed conductive layer 206, that is, the shoulder portion of the metal silicide layer 204 is removed so that a shoulder chamfer or a shoulder recess 224 is formed. Thereafter, a liner material layer 226 is formed over the substrate 200 to cover the dielectric layer 214, the cap layer 208 and the sidewall and bottom section of the funnel-shaped opening 222. The liner material layer 226 is fabricated using an insulating material such as silicon nitride or silicon oxide. The liner material layer 226 is formed, for example, by performing a chemical vapor deposition. Preferably, the liner material layer 226 is fabricated using a material that differs from a subsequently formed dielectric layer 230.

[0024] As shown in Fig. 2D, an anisotropic back etching is carried out to remove the liner material layer ~~228~~ 226 over the dielectric layer 214 and the cap layer 208 and at the bottom of the funnel-shaped opening 222. The liner material layer 226a on the sidewalls of the funnel-shaped opening 222 is retained to serve as a liner layer. Since the conductive layer 206 has a shoulder chamfer or a shoulder recess 224, the liner layer 226a at the shoulder section of the conductive layer 206 is the thickest. Thereafter, a conductive layer 228 is formed over the substrate to cover the dielectric layer 214 and the conductive structure 210 and fill the funnel-shaped opening 222. The

conductive layer 228 is fabricated using a metal material including tungsten or doped polysilicon, for example.

[0025] As shown in Fig. 2E, a chemical-mechanical polishing operation is performed to remove the conductive layer 228 above the dielectric layer 214 and the conductive structure 210. Hence, a conductive layer 228a is retained within the funnel-shaped opening ~~333~~ 222 to form a bottom plug. Thereafter, the dielectric layer 230 is formed over the substrate 200. The dielectric layer 230 has an opening 232 that exposes a portion of the bottom plug 228a. The opening 232 has a critical dimension smaller than the open end of the funnel-shaped opening 222. The dielectric layer 230 is a silicon oxide layer formed, for example, by performing a chemical vapor deposition. In general, the liner layer 226a is fabricated using a material that differs from the dielectric layer 230. Thus, even if there is some misalignment when the opening 232 is formed via a photolithographic process, the liner layer 226a may serve as an etching stop layer to prevent any over-etching in processing the dielectric layer 230.

[0027] Fig. 2F is a schematic cross-sectional view of a semiconductor device structure according to a preferred embodiment of this invention. Fig. 3 is a top view of Fig. 2F. As shown in Figs. 2F and 3, the semiconductor device comprises a plurality of conductive structures 210, a plurality of bottom plugs 228a, a plurality of top plugs 234b, a plurality of wire lines 234a, a liner layer 226a and a pair of dielectric layers 214 and 230. The conductive structures 210 are formed over a substrate 200. The bottom plugs 228a is a solid block with a funnel shape. The bottom plugs ~~228~~ 228a are

positioned between neighboring conductive structures 210 and electrically connected to the substrate 200. The liner layer 226a is set up between neighboring conductive structures 210 and the bottom plugs 228a. The top plugs 234b, which are solid blocks with a cylindrical shape, are set up over the respective bottom plugs 228a. The junction portion of the bottom plug 228a connected to the top plug 234b has a critical dimension greater than the top plug 234b. The wire lines 234a are electrically connected to respective top plugs 234b. The dielectric layer 214 is set up between the conductive structures 210 and between the bottom plugs 228a. The dielectric layer 230 is set up between the top plugs 234b and the wire lines 234a.

[0028] When this invention is applied to fabricate a memory device, the conductive structures 210 are gate structures that comprises a gate dielectric layer (not shown), a polysilicon layer 202, a metal silicide layer 204 and a cap layer ~~212~~ 208. In this case, the wire lines 234a are bit lines and the top plug 234b and the bottom plug 228a together constitute a bit line contact.